

# Rational growth of branched nanowire heterostructures with synthetically encoded properties and function

Xiaocheng Jiang<sup>a,1</sup>, Bozhi Tian<sup>a,1,2</sup>, Jie Xiang<sup>a,3</sup>, Fang Qian<sup>a,4</sup>, Gengfeng Zheng<sup>a,5</sup>, Hongtao Wang<sup>b,6</sup>, Liqiang Mai<sup>a,7</sup>, and Charles M. Lieber<sup>a,b,8</sup>

<sup>a</sup>Department of Chemistry and Chemical Biology and <sup>b</sup>School of Engineering and Applied Science, Harvard University, Cambridge, MA 02138

Contributed by Charles M. Lieber, June 2, 2011 (sent for review May 25, 2011)

Branched nanostructures represent unique, 3D building blocks for the “bottom-up” paradigm of nanoscale science and technology. Here, we report a rational, multistep approach toward the general synthesis of 3D branched nanowire (NW) heterostructures. Single-crystalline semiconductor, including groups IV, III–V, and II–VI, and metal branches have been selectively grown on core or core/shell NW backbones, with the composition, morphology, and doping of core (core/shell) NWs and branch NWs well controlled during synthesis. Measurements made on the different composition branched NW structures demonstrate encoding of functional p-type/n-type diodes and light-emitting diodes (LEDs) as well as field effect transistors with device function localized at the branch/backbone NW junctions. In addition, multibranch/backbone NW structures were synthesized and used to demonstrate capability to create addressable nanoscale LED arrays, logic circuits, and biological sensors. Our work demonstrates a previously undescribed level of structural and functional complexity in NW materials, and more generally, highlights the potential of bottom-up synthesis to yield increasingly complex functional systems in the future.

nanodevices | nanoelectronics | nanophotonics | biosensors | designed synthesis

Design and rational synthesis of semiconductor nanowire (NW) building blocks with well-defined structure and physical properties are central to the “bottom-up” approach for nanoscience and nanotechnology (1–6). To date, significant progress has been made in control of morphology, size, and composition on length scales ranging from the atomic and up (1–28). Branched or tree-like NWs, in which one or more secondary NWs grow in a radial direction from a primary NW backbone, represent an especially interesting class of NW structures because branching naturally provides access to higher dimensionality structures and the capability of achieving parallel connectivity and interconnection during synthesis (12, 13). Indeed, well-controlled variations in the composition and/or doping of backbone and branch NWs could make possible the design and realization of unique electronic and photonic nanodevices via encoding functionality synthetically at branch junctions.

Previous studies of branched NW structures have led to several advances. First, original work in 2004 (12, 13) demonstrated the controlled synthesis of Si (12), GaN (12), and GaP (13) branched NWs via a multistep nanocluster-catalyzed vapor–liquid–solid (VLS) process, in which the diameter, length, and density of nanoscale branches were defined independently from backbone NW growth. Several groups have also employed a single-step, chemical vapor transport and condensation strategy to produce a wide range of straight or twisted semiconductor branched NWs, including ZnO (14, 15), WO<sub>3</sub> (16), PbS (17), and PbSe (18). These studies have provided additional insight into growth mechanisms of branched nanostructures, but exhibited only limited control of the branch synthesis that is ultimately central to

defining functionality for device applications. More recently, the growth of branched heterostructures with different backbone and branch compositions, including ZnSe/CdSe (19) and ZnS/CdS (20, 21), was reported using a multistep approach similar to that described in 2004 (12, 13). This work showed the possibility for encoding distinct composition junctions at branch points through synthesis, but did not demonstrate the critical potential of such branch junctions to serve as electronic and optoelectronic devices. Here, we describe studies that extend in a substantial manner the synthesis of branched NW heterostructures and, significantly, that reveal well-defined electrical and optoelectronic junction properties, including the demonstration of addressable nanoscale light-emitting diode (LED) arrays, logic circuits, and biological sensors.

## Results and Discussion

We have focused on two distinct classes of branched NWs, with metal or semiconductor branches grown on either the native surface of semiconductor (type I) or on the oxide surface of core/shell semiconductor/oxide (type II) NW backbones (Fig. 1). The synthesis involves two critical steps following synthesis of the core and core/shell NWs. First, gold nanoparticles (Au-NPs) are selectively deposited onto the respective backbone surfaces using either an in situ solution reduction of AuCl<sub>4</sub><sup>-</sup> on Si-NW surfaces for type I structures or binding of Au-NPs to the oxide surfaces of Si/SiO<sub>2</sub> core/shell NWs for type II structures (see *Materials and Methods*). Transmission electron microscopy (TEM) images demonstrate that these methods provide uniformly dispersed Au-NPs on the Si (Fig. S1A) and Si/SiO<sub>2</sub> (Fig. S1C) NW surfaces, and moreover, high-resolution TEM (HRTEM) images demonstrate intimate contact between Au-NPs and the Si (Fig. S1B) and

Author contributions: X.J., B.T., L.M., and C.M.L. designed research; X.J., B.T., J.X., F.Q., G.Z., and H.W. performed research; X.J., B.T., J.X., F.Q., G.Z., H.W., L.M., and C.M.L. analyzed data; and X.J., B.T., and C.M.L. wrote the paper.

The authors declare no conflict of interest.

Freely available online through the PNAS open access option.

<sup>1</sup>X.J. and B.T. contributed equally to this work.

<sup>2</sup>Present address: Koch Institute for Integrative Cancer Research, Massachusetts Institute of Technology, Cambridge, MA 02142.

<sup>3</sup>Present address: Department of Electrical and Computer Engineering, University of California, San Diego, CA 92093.

<sup>4</sup>Present address: Department of Chemistry and Biochemistry, University of California, Santa Cruz, CA 95064.

<sup>5</sup>Present address: Laboratory of Advanced Materials and Department of Chemistry, Fudan University, Shanghai, 200438, China.

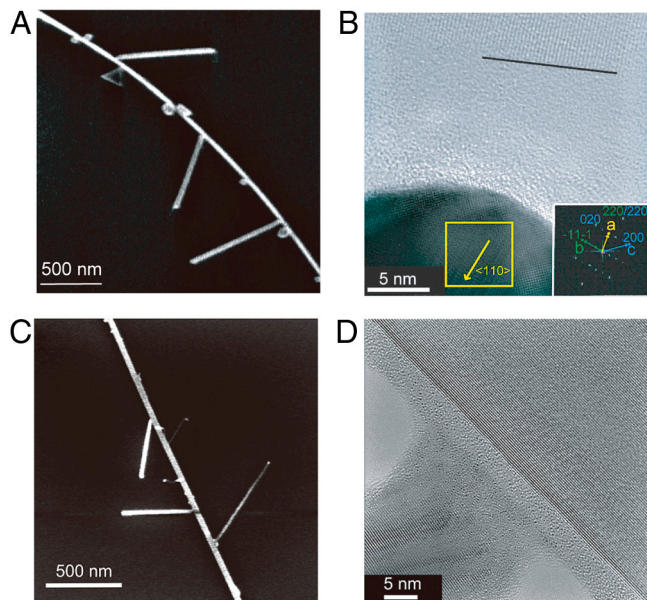
<sup>6</sup>Present address: School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, 310027, China.

<sup>7</sup>Present address: State Key Laboratory of Advanced Technology for Materials Synthesis and Processing, Wuhan University of Technology–Harvard Joint Nano Key Lab, Wuhan University of Technology, Wuhan, 430070, China.

<sup>8</sup>To whom correspondence should be addressed. E-mail: cml@cmliris.harvard.edu.

This article contains supporting information online at [www.pnas.org/lookup/suppl/doi:10.1073/pnas.1108584108/-DCSupplemental](http://www.pnas.org/lookup/suppl/doi:10.1073/pnas.1108584108/-DCSupplemental).



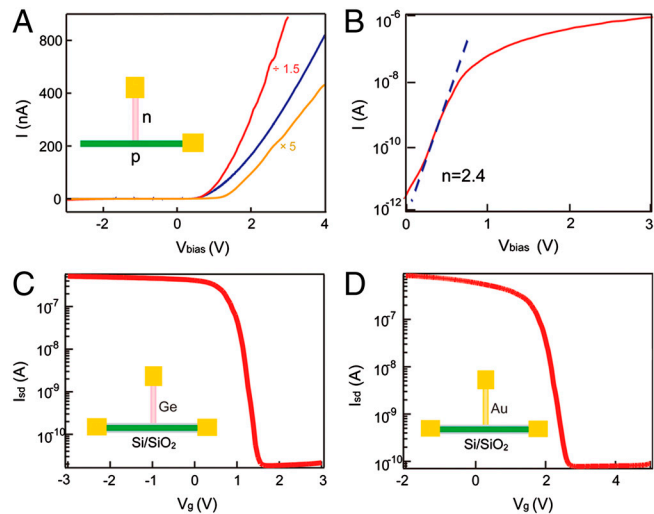


**Fig. 3.** Structural characterization of type II branched NW heterostructures. (A) SEM image of Si/SiO<sub>2</sub>/Au branched NWs. (B) HRTEM image of Si/SiO<sub>2</sub>/Au junction. The black line marks the SiO<sub>2</sub>/Si interface. (Lower Right Inset) FFT pattern from the yellow square region, indexed as a superposition of [001] (blue) and [-112] (green) zone patterns. The marked yellow spot in the FFT pattern is one of the associated double diffraction reflections, where  $a = b + c$ . (C and D) SEM (C) and HRTEM (D) images of Si/SiO<sub>2</sub>/Ge branched NW.

amorphous layer sandwiched between crystalline Si-backbone and branch NWs, which is consistent with our design for type II structures. Analysis of the Au branch last close to the junction (Fig. 3B, *Inset*) shows the superposition of  $\langle 112 \rangle$  and  $\langle 100 \rangle$  zone patterns and indicates the Au branch grows along the  $\langle 110 \rangle$  direction, the same as in Si/Au branched NWs. We note that the SiO<sub>2</sub> shell on these Si-NW backbones can be readily extended to other types of functional materials conformally deposited by atomic layer deposition (32) and has the potential to significantly expand the scope of functionalities defined at the branched junctions.

We have fabricated and measured single-branch/backbone NW devices to examine the potential for encoding of functional device properties such as p-n diodes and field effect transistors (FETs) by synthesis (see *Materials and Methods*; Fig. S3). For example, p-n diodes should be encoded at the junction of p-Si-NW backbone and n-type semiconductor branch, where we have synthesized and studied structures with n-Ge, n-GaAs, and n-CdSe branches. Two-terminal electrical transport measurements recorded on p-Si/n-Ge, p-Si/n-GaAs, and p-Si/n-CdSe backbone/branch NW structures (Fig. 4A) all exhibit clear current rectification with threshold voltages of approximately 1.0 V, consistent with expectations for p-n diode (31). More detailed characterization of the Si/GaAs p-n diode (Fig. 4B) yields a room temperature ideality factor,  $n$ , of 2.4. Although the  $n$  value indicates surface recombination in the diode (33) and suggests that further optimization could be achieved in the future, the present results nevertheless demonstrate our capability to independently define the doping profile of backbone and branch NWs necessary for encoding device function.

We have also examined the potential for encoding nanoscale FETs in type II branched NWs, where p-Si-NW backbone serves as the active semiconductor channel, the SiO<sub>2</sub> shell layer as the gate dielectric, and heavily doped n-Ge or Au-branch NWs as nanoscale gate electrodes. Source and drain contacts were defined on p-Si-NW backbone, and an additional contact was made at the end of n-Ge or Au branch as voltage input for the



**Fig. 4.** Single-branch input devices. (A) Two-terminal  $I$ - $V$  characteristics of p-n diodes encoded at p-Si/n-Ge (blue), p-Si/n-GaAs (red), and p-Si/n-CdSe (orange) branched junctions. (B)  $I$ - $V$  curve of the same p-Si/n-GaAs diode on semilog scale; the slope (blue dashed line) yields an ideality factor  $n = 2.4$ . (C and D)  $I$ - $V$  curves of nanoscale FETs encoded at p-Si/SiO<sub>2</sub>/n-Ge (C) and p-Si/SiO<sub>2</sub>/Au (D) branched junctions, respectively. A source-drain voltage of 0.5 V was used in the measurement.

gate electrode (Fig. 4C, *Inset*, and D, *Inset* and Fig. S3B and C). Current ( $I_{sd}$ ) vs. branch-gate voltage ( $V_g$ ) data recorded on p-Si/SiO<sub>2</sub>/n-Ge (Fig. 4C) and p-Si/SiO<sub>2</sub>/Au (Fig. 4D) branched NW FETs at a source-drain voltage of 0.5 V show a characteristic depletion mode FET behavior (31), with a turnoff current  $< 100$  pA and on/off ratio  $> 10^4$ . The calculated subthreshold slopes for these two nanoscale FET devices are 120 and 150 mV/decade, respectively. The subthreshold values, which indicate good gate coupling, are especially notable given that the gate lengths for the n-Ge and Au-branch devices are only 30 and 35 nm, respectively.

In addition, we have investigated additional functional properties for synthetically encoded branch/backbone NW structures as well as the incorporation of multiple functional branches. First, we have characterized the photonic properties of p-Si/n-GaAs backbone/branch heterostructures, where the direct-band-gap GaAs branch can yield light emission in a forward biased diode (34). Significantly, electroluminescence (EL) data recorded from a p-Si/n-GaAs device (Fig. 5A) exhibits highly localized emission from the branch junction in forward bias, thus making these point-like, nanoscale active emitters (nanoLEDs). The EL spectrum (Fig. 5A, *Lower*) exhibits a peak maximum at 860 nm, corresponding to the GaAs band-edge emission. We note that the localized emission from the branch junctions was robust; that is, repeated on/off cycles did not affect the emission properties, and studies of over 20 p-Si/n-GaAs nanoLEDs yielded similar results.

We have exploited the reproducibility and robustness of the p-Si/n-GaAs nanoLEDs to study an addressable array consisting of three n-GaAs NW branches on p-Si-NW backbone (Fig. 5B). When a forward bias was applied to turn on one (Fig. 5B, *Upper Right*), two (Fig. 5B, *Lower Left*), or three (Fig. 5B, *Lower Right*) nanoLEDs sequentially, EL measurements demonstrate localized and addressable emission only from the junctions in forward bias. Moreover, we have assembled and characterized seven robust nanoLEDs within a  $100 \times 100 \mu\text{m}^2$  area (Fig. S4), thus demonstrating the potential of this bottom-up approach for larger-scale integration of these unique photonic devices.

In addition, the concept of synthetically encoding multiple functional branch devices has been used to investigate their potential as logic gates. A two branch input FET configured from



**Synthesis of Si/semiconductor and Si/SiO<sub>2</sub>/semiconductor branched NWs.** Si or Si/SiO<sub>2</sub> NWs with deposited Au-NPs were dispersed on SiO<sub>2</sub> surface of heavily Si substrates as above and then immediately placed into the appropriate NW gas phase growth system to prepare branched semiconductor NWs. Ge branches were grown at 290 °C, 200 torr for 15 min, with the flow of 10 sccm GeH<sub>4</sub> (10%), 10 sccm PH<sub>3</sub> (1,000 ppm in H<sub>2</sub>), and 200 sccm H<sub>2</sub> as described previously (41). The growth of other III-V and II-VI branches was achieved by thermal evaporation and vapor transport method (42). Powders with the same composition were put into the center of the quartz tube, which was heated to 650–780 °C, while the branch growth temperature was approximately 400–600 °C. 30 sccm of H<sub>2</sub> was used as the carrier gas, and pressure was kept at 40 torr.

**Device Fabrication and Measurement.** Single- and multiple-branch input devices were fabricated on SiO<sub>2</sub> surface of Si substrates (50-nm thermal oxide, n-type 0.005 Ω-cm, Nova Electronic Materials) using electron beam lithography (43) followed by thermal evaporation of metals. Ti/Pd (5/50 nm) contacts were used for both Si and Ge NWs; Ti/Al/Pd/Au (20/80/20/30 nm) contacts were used for other III-V and II-VI semiconductor NWs. Current-voltage (*I*-*V*) data were recorded using an Agilent semiconductor parameter analyzer (Model 4156C) with contacts to devices made using a probe station (Desert Cryogenics, Model TTP4). EL from branched NW structures was characterized with a homebuilt microluminescence instrument (44). Arrays of Si/Au-NP NW devices were defined by photolithography (37). Ti/Pd (5/50 nm) metal contacts were deposited by thermal evaporation and then passivated by subsequent deposition of 50-nm thick Si<sub>3</sub>N<sub>4</sub> coating (37). The completed device chip was subject to Au-branch growth as described above.

The Au branches were modified in two steps. First, the devices were reacted with a 10 mg/mL solution of DMSO (Sigma-Aldrich) for approximately 4 h, followed by extensive rinsing with DMSO. Anti-PSA (Abl, clone ER-PR8, Neo-Markers) was then coupled to the succinimidyl(NHS)-terminated Au branches surfaces by reaction of 10–20 μg/mL antibody in a pH 8.4, 10 mM phosphate buffer solution for a period of 2–4 h. Unreacted NHS groups were subsequently passivated by reaction with ethanolamine under similar conditions. PSA and BSA protein samples in 1 μM phosphate buffer solution (pH, 7.4) were flowed under a flow rate of 0.30–0.60 mL/h through the microfluidic channel while monitoring the branch nanowire device properties as described in detail elsewhere (37).

**Stress Field Simulation.** Stress field simulations were carried out using finite element method (ABAQUS software, version, 6.5-1). To simulate the stress in Si/GaAs branched structure, we took the axis of GaAs branch and Si backbone as (111) and (211), respectively, and the following material constants are used: modulus of elasticity,  $c_{11(\text{GaAs})} = 1.18 \times 10^{11}$  Pa,  $c_{12(\text{GaAs})} = 0.538 \times 10^{11}$  Pa,  $c_{44(\text{GaAs})} = 0.594 \times 10^{11}$  Pa,  $c_{11(\text{Si})} = 1.662 \times 10^{11}$  Pa,  $c_{12(\text{Si})} = 0.664 \times 10^{11}$  Pa,  $c_{44(\text{Si})} = 0.798 \times 10^{11}$  Pa; lattice constant,  $a_{(\text{Si})} = 0.543$  nm,  $a_{(\text{GaAs})} = 0.565$  nm; backbone to branch width ratio, 2:1.

**ACKNOWLEDGMENTS.** We thank Profs. R. Gordon and F. Spaepen and Drs. H. Yan, Y. Dong, J. Huang, Y. Wu, B. Timko, and Y. Fang for helpful discussions and constructive comments on the manuscript. C.M.L. acknowledges support of this work by the Air Force Office of Scientific Research and a National Security Science and Engineering Faculty Fellow award.

- Hu J, Odom T, Lieber CM (1999) Chemistry and physics in one dimension: Synthesis and properties of nanowires and nanotubes. *Acc Chem Res* 6:435–445.
- Lieber CM (2003) Nanoscale science and technology: Building a big future from small things. *MRS Bull* 28:486–491.
- Li Y, Qian F, Xiang J, Lieber CM (2006) Nanowire electronic and optoelectronic devices. *Mater Today* 9:18–27.
- Law M, Goldberger J, Yang PD (2004) Semiconductor nanowires and nanotubes. *Annu Rev Mater Res* 34:83–122.
- Thelander C, et al. (2006) Nanowire-based one-dimensional electronics. *Mater Today* 9:28–35.
- Wang ZL (2004) Functional oxide nanobelts: Materials, properties and potential applications in nanosystems and biotechnology. *Annu Rev Phys Chem* 55:159–196.
- Gudiksen MS, Lauhon LJ, Wang J, Smith DC, Lieber CM (2002) Growth of nanowire superlattice structures for nanoscale photonics and electronics. *Nature* 415:617–620.
- Wu Y, Fan R, Yang P (2002) Block-by-block growth of single-crystalline Si/SiGe superlattice nanowires. *Nano Lett* 2:83–86.
- Bjork MT, et al. (2002) One-dimensional heterostructures in semiconductor nanowires. *Appl Phys Lett* 80:1058–1060.
- Lauhon LJ, Gudiksen MS, Wang D, Lieber CM (2002) Epitaxial core-shell and core-multi-shell nanowire heterostructures. *Nature* 420:57–61.
- Tian B, Xie P, Kempa TJ, Bell DC, Lieber CM (2009) Single crystalline kinked semiconductor nanowire superstructures. *Nat Nanotechnol* 4:824–829.
- Dick KA, et al. (2004) Synthesis of branched 'nanotrees' by controlled seeding of multiple branching events. *Nat Mater* 3:380–384.
- Wang D, Qian F, Yang C, Zhong ZH, Lieber CM (2004) Rational growth of branched and hyperbranched nanowire structures. *Nano Lett* 4:871–874.
- Gao P, Wang ZL (2002) Self-assembled nanowire-nanoribbon junction arrays of ZnO. *J Phys Chem B* 106:12653–12658.
- Yan HQ, He RR, Pham J, Yang PD (2003) Morphogenesis of one-dimensional ZnO nano- and microcrystals. *Adv Mater* 15:402–405.
- Zhou J, et al. (2005) Three-dimensional tungsten oxide nanowire networks. *Adv Mater* 17:2107–2110.
- Bierman MJ, Lau YKA, Kvit AV, Schmitt AL, Jin S (2008) Dislocation-driven nanowire growth and Eshelby Twist. *Science* 320:1060–1063.
- Zhu J, et al. (2008) Formation of chiral branched nanowires by the Eshelby Twist. *Nat Nanotechnol* 3:477–481.
- Dong A, Tang R, Buhro WE (2007) Solution-based growth and structural characterization of homo- and heterobranched semiconductor nanowires. *J Am Chem Soc* 129:12254–12262.
- Jung Y, Ko DK, Agarwal R (2007) Synthesis and structural characterization of single-crystalline branched nanowire heterostructures. *Nano Lett* 7:264–268.
- Zhou W, et al. (2008) Controllable fabrication of high-quality 6-fold symmetry-branched CdS nanostructures with ZnS nanowires as templates. *J Phys Chem C* 112:9253–9260.
- Milliron DJ, et al. (2004) Colloidal nanocrystal heterostructures with linear and branched topology. *Nature* 430:190–195.
- Dick KA, et al. (2006) Position-controlled interconnected InAs nanowire networks. *Nano Lett* 6:2842–2847.
- Suyatin DB, et al. (2008) Electrical properties of self-assembled branched InAs nanowire junctions. *Nano Lett* 8:1100–1104.
- Gautam UK, Fang X, Bando Y, Zhan J, Golberg D (2008) Synthesis, structure, and multiply enhanced field-emission properties of branched ZnS nanotube-In nanowire core-shell heterostructures. *ACS Nano* 2:1015–1021.
- Meng G, et al. (2009) A general synthetic approach to interconnected nanowire/nanotube and nanotube/nanowire/nanotube heterojunctions with branched topology. *Angew Chem Int Ed Engl* 48:7166–7170.
- Chen B, et al. (2010) Crystalline silicon nanotubes and their connections with gold nanowires in both linear and branched topologies. *ACS Nano* 4:7105–7112.
- Jun K, Jacobson JM (2010) Programmable growth of branched silicon nanowires using a focused ion beam. *Nano Lett* 10:2777–2782.
- Johnson CJ, Dujardin E, Davis SA, Murphy CJ, Mann S (2002) Growth and form of gold nanorods prepared by seed-mediated, surfactant-directed synthesis. *J Mater Chem* 12:1765–1770.
- Morales AM, Lieber CM (1998) A laser ablation method for the synthesis of crystalline semiconductor nanowires. *Science* 279:208–211.
- Sze SM (1981) *Physics of Semiconductor Devices* (Wiley, New York).
- Hausmann DM, Kim E, Becker J, Gordon RG (2002) Atomic layer deposition of hafnium and zirconium oxides using metal amide precursors. *Chem Mater* 14:4350–4358.
- Mzhar B, Morkoc H (1993) Surface recombination in GaAs PN junction diode. *J Appl Phys* 73:7509.
- Huang Y, Duan X, Lieber CM (2005) Nanowires for integrated multicolor nanophotonics. *Small* 1:142–147.
- Huang Y, et al. (2001) Logic gates and computation from assembled nanowire building blocks. *Science* 294:1313–1317.
- Cui Y, Wei Q, Park H, Lieber CM (2001) Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science* 293:1289–1292.
- Zheng G, Patolsky F, Cui Y, Wang WU, Lieber CM (2005) Multiplexed electrical detection of cancer markers with nanowire sensor arrays. *Nat Biotechnol* 23:1294–1301.
- Patolsky F, Lieber CM (2005) Nanowire nanosensors. *Mater Today* 8:20–28.
- Wu Y, et al. (2004) Controlled growth and structures of molecular-scale silicon nanowires. *Nano Lett* 4:433–436.
- Sun XH, et al. (2001) Surface reactivity of Si nanowires. *J Appl Phys* 89:6396–6399.
- Greytak AB, Lauhon LJ, Gudiksen MS, Lieber CM (2004) Growth and transport properties of complementary germanium nanowire field-effect transistors. *Appl Phys Lett* 84:4176–4178.
- Jiang X, et al. (2007) "InAs/InP radial nanowire heterostructures as high electron mobility devices". *Nano Lett* 7:3214–3218.
- Cui Y, Zhong Z, Wang D, Wang WU, Lieber CM (2003) High performance silicon nanowire field effect transistors. *Nano Lett* 3:149–152.
- Qian F, Gradedcak S, Li Y, Wen Y, Lieber CM (2005) Core/multishell nanowire heterostructures as multicolor, high-efficiency light-emitting diodes. *Nano Lett* 5:2287–2291.